Secondment report

TIRAMISU DC1.1

Fellow:	Ashwin Santhosh
Research project title:	“Reliable RISC-V based Architectures for Edge AI”
From:	TUT
To:	IFAG
Secondment period:	10.10.2025 – 18.12.2025

Activities during the secondment

Scope and objectives

- Training on the Metagen automation framework and Cadence Xcelium simulation environment.
- Practical understanding of the SBST flow, including fault injection and PFC.
- Research on fault localization in a RISC-V processor using intermediate checks.
- A collaborative research paper with Infineon.

Activities

- Hands-on training on the Metagen automation framework and Cadence Xcelium simulation environment.
- Study and practical application of the SBST flow, including SBST execution, fault injection, and PFC-based detection.
- Experimental research on fault localization in a RISC-V processor using intermediate checks.

Main results achieved

- Working knowledge of Metagen, Cadence Xcelium, and the SBST flow was acquired.
- Fault localization using intermediate checks was demonstrated on a RISC-V processor.
- SBST pattern IDs responsible for fault activation were identified, reducing the fault search space and enabling runtime fault detection.

Next steps

- Automate the fault localization approach and further refine localization to fewer candidate signals.
- Complete experimental evaluation, consolidate results, and prepare a collaborative research paper with Infineon.

Self-evaluation

Overall score

I consider this secondment successful, with regard to the research objectives achieved, skills developed, supervision quality and diversity of the resources. (Agree = 5 … Disagree = 1)

5

Optional comments

None

Date of the report approval by the supervisor: 12.01.2026

The TIRAMISU Doctoral Network has received funding from the European Union’s Horizon Europe research and innovation programme under the Marie Skłodowska-Curie grant agreement No 101169378.